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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,359	11/18/2003	Sudip K. Nag	X-1376 US	8181

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/717,359	NAG, SUDIP K.
	Examiner	Art Unit
	Vuthe Siek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/717,359 filed on 11/18/2003. Claims 1-20 remain pending in the application.

Claim Objections

2. Claims 1, 8, 15, 17 and 19 are objected to because of the following informalities: "timing attributes" and "timing parameters", needed to be clarified to be more concise; "may be" should be replaced with a concise claimed language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Srinivasan et al. (US 2004/0196081 A1).

5. As to claim 1, Srinivasan et al. teach a method for forming timing parameters for a circuit design having a predefined routing topology within an integrated circuit (IC) comprising determining sets of timing attributes for the routing topology (delays for clock tree, each cluster, block, being placed and routed within integrated circuit design),

each set being associated with one of a plurality of locations within the IC in which the circuit design will be placed; forming timing parameters (minimum and maximum delay) in response to the sets of timing attributes; and associating the timing parameters with the routing topology (a balanced routing topology for each of the clusters) (Fig. 5, 9, 12, [0075-0079, 0086-0089]).

6. As to claims 2, Srinivasan et al. teach the routing topology comprising a source and at least on sink, and wherein the each of set of timing attributes comprising a signal delay between each source-sink pair (delay between source-sink pair whether within clock tree, cluster, or block placed within the IC) (0078, 0086-0088).

7. As to claim 3, Srinivasan et al. teach selecting a minimum delay in response to the signal delay for each source-sink pair in the set of the timing attributes; and selecting a maximum delay in response to the signal delay for each source-sink pair in each set of timing attributes (0078, 0086-0089).

8. As to claims 4-5, Srinivasan et al. teach the source provides a clock signal to the at least on sink and wherein each set of timing attributes further comprising a clock skew for each source-sink pair; and the forming further comprising selecting a maximum skew in response to the clock skew for each source-sink pair in each set of the timing attributes (Fig. 5, 9, 12; 0078, 0086-0089).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6-20 are rejected under 35 U.S.C. 103(a) as being obvious over Srinivasan et al. in view of the applicant admitted prior art (see background of the invention).

11. As to claims 6-7 and 13-14, Srinivasan et al. teach an IC designed method that provides a balanced routing topology for each of clusters including clock tree having one or more clusters being placed within each of the blocks to thereby providing a balanced routing topology of the entire IC design . The admitted prior art discloses the IC design is a programmable logic device, where each of the plurality of locations is defined by a group of the programmable logic blocks. Utilizing the method as taught by Srinivasan et al. in an IC design that is a programmable logic device would have been obvious to one of practitioners in the art because it would provide a balanced routing topology for each of the clusters (each group of programmable logic blocks) within each of placement locations.

12. As to claims 8, 15, 17 and 19, Srinivasan et al. teach a method for forming timing parameters for a circuit design having a predefined routing topology within an integrated circuit (IC) comprising determining sets of timing attributes for the routing topology (delays for clock tree, each cluster, block, being placed and routed within integrated circuit design), each set being associated with one of a plurality of locations within the IC in which the circuit design will be placed; forming timing parameters (minimum and maximum delay) in response to the sets of timing attributes; and associating the timing

parameters with the routing topology (a balanced routing topology for each of the clusters) (Fig. 5, 9, 12, [0075-0079, 0086-0089]). Srinivasan et al. teach routing topology, except a template having a predefined routing topology. Since a template based routing topology would facilitate routing topology process, it would have been obvious to one of ordinary skill in the art to perform routing topology based on template of predefined routing topology in order to save time and would be cost effective.

13. As to claim 9, remarks set forth in rejecting claim 2 apply because of similar claimed limitations.

14. As to claim 10, remarks set forth in rejecting claim 3 apply because of similar claimed limitations.

15. As to claim 11, remarks set forth in rejecting claim 4 apply because of similar claimed limitations.

16. As to claim 12, remarks set forth in rejecting claim 5 apply because of similar claimed limitations.

17. As to claim 13, remarks set forth in rejecting claim 2 apply because of similar claimed limitations.

18. As to claims 16, 18 and 20, Srinivasan et al. teach placing and routing and analyzing the IC design (Fig. 5 ,9, 12; 0087-0089).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER